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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02079686.8

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Circuit arrangement

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Circuit arrangement

The invention relates to a circuit arrangement for operating a high pressure discharge lamp comprising

- input terminals for connection to a supply voltage source,
- a DC-DC-converter coupled to the input terminals for generating a DC current out of a supply voltage supplied by the supply voltage source and comprising
  - a control loop for controlling the DC current at a value that is represented by a reference signal Sref,
  - a control circuit for adjusting the reference signal Sref, and
  - an output capacitor,
- a commutator for commutating the polarity of the DC current and comprising lamp connection terminals and an ignition inductor.

Such a circuit arrangement is known and is for instance often used to operate ultra high pressure lamps in projection equipment. In practice the frequency of commutation is in the order of magnitude of 10 Hz. Between two subsequent commutations the DC current is controlled at a constant value represented by the reference value Sref for most of the time. As a consequence the current through the high pressure discharge lamp is a low frequency substantially square wave shaped AC current. It has been found that the high pressure discharge lamp can be operated in a very efficient way by means of such a current. A problem associated with the circuit arrangement is that a commutation of the polarity of the DC current effects a substantially stepwise change in the load of the circuit arrangement. This stepwise change in the load of the circuit arrangement causes the down converter output capacitor to resonate with the ignition inductor. This resonance in turn often causes audible noise and influences the light output of the lamp. Furthermore this resonance can shorten the life time of the lamp. In practice this resonance is often counteracted by temporarily decreasing the value of Sref in the direct vicinity of a commutation. The decrease in Sref, often referred to as "dip", causes the DC-current to temporarily have a comparatively low value during a small time lapse in which commutation takes place. As a result the resonance caused by the stepwise load change is suppressed to a large extent. The dip can be considered

as a modulation of the reference signal Sref that is taking place with the same frequency as the modulation of the DC-current. The "dip" is characterized by dip parameters such as ΔSref (the depth of the dip), the time lapse during which Sref is maintained at the decreased level, the rate at which Sref is decreased at the beginning of the dip, the rate at which Sref is increased at the end of the dip and the phase relation between the modulated signal Sref and the lamp current. It has been found in practice that different types of high pressure lamps require a different setting of the dip parameters in order to obtain a maximal suppression of the resonance. Similarly, it has also been found that high pressure discharge lamps of the same type but with a different "age" (= number of hours that the lamp has burned), require a different setting of the dip parameters for an optimal suppression of the resonance. As a consequence the resonance suppression implemented in the known circuit arrangements is only optimized for one particular lamp type and even only for one particular age of that lamp.

The invention aims to provide a circuit arrangement for operating a high pressure discharge lamp in which an effective suppression of the resonance between the output capacitor of the DC-DC-converter and the ignition inductor is realized for many different types of high pressure discharge lamps during their complete life time.

A circuit arrangement as mentioned in the opening paragraph is therefore according to the invention characterized in that the control circuit comprises means for adjusting the reference signal in dependency of the peak amplitude of an AC voltage that is present across the output capacitor and is caused by the commutation of the DC current.

In a circuit arrangement according to the invention the setting of at least part of the dip parameters is controlled in dependency of the amplitude of the AC voltage that is present over the output capacitor and that is caused by a resonance between the output capacitor of the DC-DC-converter and the ignition inductor. As a consequence the setting of at least part of the dip parameters is continuously adjusted in such a way that an optimal suppression of the resonance results. It has been found that in a circuit arrangement according to the invention the resonance is effectively suppressed for many different types of high pressure discharge lamps. It has also been found that this effective suppression of the resonance was maintained during the whole life time of the lamp.

In a first preferred embodiment of a circuit arrangement according to the invention, the control circuit comprises circuitry for generating a signal Sring that represents the peak amplitude of the AC voltage over the output capacitor and circuitry for subtracting the signal Sring from the reference signal Sref. The control circuit in this first preferred

embodiment is comparatively simple and can also be implemented in a comparatively simple way. The circuitry for generating the signal Sring may comprise a filter that passes a frequency band around the frequency of the resonance. Preferably the circuitry for generating the signal Sring comprises a peak detector coupled to the output capacitor.

In a second preferred embodiment of a circuit arrangement according to the invention, the control circuit comprises

- a first circuit part for generating a signal Sring that represents the peak amplitude of the AC voltage over the output capacitor,
- a second circuit part for modulating the reference signal Sref at a modulation frequency that equals the frequency of the commutation of the DC current by subsequently
  - decreasing the reference signal Sref by an amount ΔSref during a first time interval Δt1 that starts a second time interval Δt2 before each commutation of the DC current,
  - maintaining the reference signal at the decreased value during a third time interval Δt3,
  - increasing the reference signal Sref by an amount ΔSref during a fourth time interval Δt4
- a third circuit part for adjusting at least one parameter chosen from the group formed by ΔSref, Δt1, Δt2, Δt3 and Δt4 so that the amplitude of the signal Sring is minimal.

The third circuit part in this second preferred embodiment allows a very precise control of one or more of the dip parameters resulting in a very effective suppression of the resonance. The adjusting of the one or more dip parameters is preferably done by means comprised in the third circuit part for increasing and decreasing the value of the parameter until the amplitude of the signal Sring is minimal. Although the adjustment of only one of the parameters until the amplitude of Sring is minimal effects a certain suppression of the resonance, it is preferred that the third circuit part comprises means for adjusting at least 2 parameters chosen from the group formed by ΔSref, Δt1, Δt2, Δt3 and Δt4 so that the amplitude of the signal Sring is minimal.

Good results have been obtained for embodiments, wherein the third circuit part comprises means for adjusting the parameters ΔSref, Δt2 and Δt3 so that the amplitude of the signal Sring is minimal. The adjustment of the parameters is preferably effected by means of a microcontroller.

Embodiments of a circuit arrangement according to the invention will be explained making reference to a drawing. In the drawing

Fig. 1 shows a first embodiment of a circuit arrangement according to the invention, with a lamp connected to it;

Fig. 2 shows a second embodiment of a circuit arrangement according to the invention with a lamp connected to it, and

Fig. 3 shows the shape of the modulated signal Sref and the current through the lamp in the second embodiment as a function of time.

In Fig. 1, K1 and K2 are input terminals for connection to a supply voltage source. Input terminals K1 and K2 are connected by means of a series arrangement of a switching element Sd, an inductive element L1, an output capacitor Cout and an ohmic resistor R3. A common terminal of output capacitor Cout and ohmic resistor R3 is connected to a common terminal of switching element Sd and inductor L1 by means of a diode D1. CSG is a circuit part for generating a control signal for alternately rendering switching element Sd conductive and non-conductive. An output terminal of circuit part CSG is coupled to a control electrode of switching element Sd. A first input terminal of circuit part CSG is coupled to input terminal K2. A second input terminal of circuit part CSG is connected to an output terminal of circuit part ADD. Circuit part ADD is a circuit part for generating at its output terminal a signal that is the sum of a first signal present at a first input terminal of circuit part ADD and a second signal present at a second input terminal of circuit part ADD. The first input terminal of circuit part ADD is connected to an output terminal of circuit part Srefgen. Circuit part Srefgen is a circuit part for generating a reference signal Sref. A common terminal of inductive element L1 and output capacitor Cout is connected to an input terminal of peak detector PD. An output terminal of peak detector PD is connected to a first input terminal of operational amplifier AMP by means of an ohmic resistor R1. A second input terminal of operational amplifier AMP is connected to ground potential. An output terminal of operational amplifier AMP is connected to the first input terminal of operational amplifier AMP by means of an ohmic resistor R2. The output terminal of operational amplifier AMP is also directly connected to the second input terminal of circuit part ADD. The operational amplifier AMP and ohmic resistors R1 and R2 together form an integrator. Switching element Sd, circuit part CSG, inductive element L1, output capacitor Cout, diode D1, ohmic resistor R3, peak detector PD, the integrator, circuit part Srefgen and circuit part ADD together form a DC-DC-converter for generating a DC current out of a

supply voltage supplied by the supply voltage source. In the embodiment shown in Fig. 1 this DC-DC-converter is of the down-converter type. Circuit part Srefgen, ohmic resistor R3 and part of the contents of circuit part CSG together form a control loop for controlling the DC current at a value that is represented by the reference signal Sref. Peak detector PD, the integrator and circuit part ADD together form a control circuit for adjusting the reference signal Sref. Peak detector PD, the integrator and circuit part ADD together also form means for adjusting the reference signal in dependency of the amplitude of an AC voltage that is present across the output capacitor and is caused by the commutation of the DC current. Peak detector PD forms circuitry for generating a signal Sring that represents the peak amplitude of the AC voltage over the output capacitor Cout. The integrator is laid out in such a way that the signal present at its output has the absolute value of Sring but a polarity that is opposite to the polarity of the signal Sref. For this reason the circuit part ADD generates at its output terminal a signal that equals Sref – Sring. Therefor the integrator together with the circuit part ADD forms circuitry for subtracting the signal Sring from the reference signal Sref.

Output capacitor Cout is shunted by a series arrangement of switching element S1 and switching element S2 and also by a series arrangement of switching element S3 and switching element S4. A common terminal of switching element S1 and switching element S2 is connected to a common terminal of switching element S3 and switching element S4 by means of a series arrangement of ignition inductor Lign and capacitor Cres. Capacitor Cres is shunted by an ultra high pressure discharge lamp LA connected to lamp connection terminals K3 and K4 situated at respective sides of capacitor Cres. Control electrodes of the switching elements S1-S4 are coupled to respective output terminals of a circuit part BC for generating control signals for controlling the conductive state of switching elements S1-S4. In fig. 1 this coupling is indicated by means of dotted lines. Switching elements S1-S4, circuit part BC, ignition inductor Lign, lamp terminals K3 and K4 and capacitor Cres together form a commutator for commutating the polarity of the DC current generated by the DC-DC-converter.

The operation of the circuit arrangement shown in Fig. 1 is as follows.

When the input terminals K1 and K2 are connected to a supply voltage source that in case of the embodiment shown in Fig. 1 supplies a DC supply voltage, the circuit part CSG generates a control signal that renders the switching element Sd alternately conductive and non-conductive at a high frequency, for instance 35 kHz. As a result a DC voltage with a lower amplitude than the DC supply voltage is present over the output capacitor Cout, while a DC current is supplied to the commutator. The circuit part BC controls the switches S1-S4

alternately in two different states. In the first state the switching elements S1 and S4 are conductive and the switching elements S2 and S3 are non-conductive. In the second state the switching elements S2 and S3 are conductive and the switching elements S1 and S4 are non-conductive.

When the lamp has not yet ignited, the frequency at which the circuit part BC changes the state of the switches S1-S4 is comparatively high, so that the ignition inductor resonates with the capacitor Cres. As a result a comparatively high voltage is present across capacitor Cres that ignites the lamp. After ignition of the lamp the frequency at which the circuit part BC changes the state of the switches S1-S4 is comparatively low, for instance 90 Hz. As a result the lamp current is a low frequency substantially square wave shaped AC current. For a very short time lapse between the two states all the switching elements are maintained in the non-conductive state to prevent the switching elements that are part of the same series arrangement to become conductive at the same time and thereby forming a short circuit. During this very short time lapse the load of the DC-DC-converter is zero. Before and after this very short time lapse the load of the DC-DC-converter differs from zero. The abrupt change in the load taking place during commutation causes the output capacitor Cout and the ignition inductor to resonate. Between commutations, when there is no resonance between the output capacitor Cout and the ignition inductor Lign and thus no AC voltage present across the output capacitor Cout, the signal at the second input terminal of circuit part ADD is approximately equal to zero. The signal present at the output terminal of circuit part ADD and also at the first input terminal of circuit part CSG therefore equals Sref. The voltage over ohmic resistor R3 represents the actual value of the DC current generated by the DC-DC-converter and is present at the second input terminal of circuit part CSG. A comparator comprised in the circuit part CSG compares the signals present at the input terminals of the circuit part CSG and generates an error signal that influences the frequency and/or the duty cycle of the control signal generated by the circuit part CSG in such a way that the DC current is maintained at a value that corresponds to the value of the reference signal Sref. When the output capacitor Cout and the ignition inductor Lign resonate as a result of a commutation, an AC voltage is present across output capacitor Cout. The peak detector PD generates a signal Sring that represents the peak amplitude of the AC voltage that is present across the output capacitor Cout and is present at the second input terminal of circuit part ADD. As explained hereabove the integrator is laid out in such a way that the signal present at the second input terminal of circuit part ADD equals signal Sring in magnitude but has a polarity that is opposite to the polarity of the signal Sring and the signal Sref. As a

consequence the signal present at the output of circuit part ADD equals Sref – Sring. The value of the signal present at the first input terminal of circuit part CSG is thus decreased and as a result of that the amplitude of the DC current generated by the DC-DC-converter is also decreased. As a consequence the resonance between the output capacitor Cout and the ignition inductor Lign is effectively suppressed. Since the extent to which the DC current is decreased is directly influenced by the peak amplitude of the AC voltage across output capacitor Cout, the decrease in current is automatically adjusted for different lamp types to a value that corresponds to maximal resonance suppression. Similarly, when a lamp of a certain type ages, the decrease in DC current is also adjusted automatically to realize an effective suppression of the resonance during the whole life time of the lamp.

In Fig. 2, components and circuit parts that are similar to components and circuit parts of the circuit arrangement shown in Fig. 1 are labeled in the same way. The topology of the circuit arrangement shown in Fig. 2 differs from that of the circuit arrangement in Fig. 1 in that the integrator formed by the operational amplifier AMP and the ohmic resistors R1 and R2 has been replaced by a microprocessor μP. The microprocessor μP together with circuit part ADD forms a second circuit part for modulating the reference signal Sref at a modulation frequency that equals the frequency of the commutation of the DC current by subsequently decreasing the reference signal Sref by an amount ΔSref during a first time interval Δt1 that starts a second time interval Δt2 before each commutation of the DC current, maintaining the reference signal at the decreased value during a third time interval Δt3, and increasing the reference signal Sref by an amount ΔSref during a fourth time interval Δt4.

The microprocessor μP also forms a third circuit part for adjusting at least one parameter chosen from the group formed by ΔSref, Δt1, Δt2, Δt3 and Δt4 so that the amplitude of the signal Sring is minimal. In the embodiment shown in Fig. 2 the microprocessor comprises means for adjusting the parameters ΔSref, Δt2 and Δt3 so that the amplitude of the signal Sring is minimal.

The operation of the circuit arrangement shown in Fig. 2 is as follows. During stationary operation of the circuit arrangement the DC-DC-converter and the commutator operate in the same way as in the circuit arrangement shown in Fig. 1. Similar to the peak detector PD comprised in the circuit arrangement in Fig. 1, the peak detector PD comprised in the circuit arrangement in Fig. 2 generates a signal Sring that represents the peak amplitude of the AC voltage over the output capacitor Cout. The microprocessor μP

generates a modulation signal and together with the circuit part ADD modulates the reference signal Sref with a frequency that equals the commutation frequency by subsequently decreasing the reference signal Sref by an amount ΔSref during a first time interval Δt1 that starts a second time interval Δt2 before each commutation of the DC current, maintaining the reference signal at the decreased value during a third time interval Δt3, and increasing the reference signal Sref by an amount ΔSref during a fourth time interval Δt4. The resulting shape of the modulated reference signal is shown in Fig. 3. It can be seen that the value of Sref is constant most of the time but the modulation results in a periodical temporary decrease of the reference signal Sref. These periodical decreases start at a time interval Δt2 before commutation and have a shape that is determined by the parameters ΔSref, Δt1, Δt1 and Δt4. Fig. 3 also shows the shape of the lamp current as a function of time. The lamp current has a constant amplitude most of the time. A time lapse Δt2 before each commutation the amplitude decreases during the time interval Δt1. The amplitude of the lamp current is then maintained at a constant value during the time interval Δt3. In the course of the time interval Δt3 the commutation of the DC current is taking place. After the time interval Δt3 the amplitude of the lamp current increases back to its original value during the time interval Δt4. It is noteworthy that Δt1 is not necessarily equal to Δt4 and that commutation does not necessarily take place when half of the time interval Δt3 has lapsed but may take place at any other time in the time interval Δt3 depending on for instance the value of Δt2.

During operation of the circuit arrangement, the microprocessor adjusts the values of the parameters ΔSref, Δt2 and Δt3 continuously in the following way. The value of the signal Sring is saved in a memory. Subsequently parameter ΔSref is increased by a predetermined amount and the value of the signal Sring after the increase of ΔSref is compared with the value before the increase that was saved in the memory. In case the signal Sring is decreased as a result of the increase of ΔSref, the new value of Sring is saved in the memory by overwriting the previous value and ΔSref is increased once more by the predetermined amount. This procedure is repeated until an increase in ΔSref causes the signal Sring to increase. In the latter case ΔSref is decreased by the predetermined amount and the resulting value of Sring is saved in the memory by overwriting the previous value. In case the first increase of ΔSref causes an increase in the signal Sring the microprocessor decreases the value ΔSref until a further decrease causes an increase in the signal Sring. The signal Sring is thus minimized by adjusting the parameter ΔSref. The microprocessor

subsequently increases and decreases the parameter Δt2 until a minimal value of the signal Sring results, in the same way as outlined hereabove for the parameter ΔSref. After the adjustment of parameter Δt2, parameter Δt3 is adjusted at a value corresponding to a minimal value of the signal Sring. After the adjustment of parameter Δt3 the microprocessor subsequently adjusts ΔSref, Δt2 and Δt3 again etc. Because of the continuous adjustment of the parameters ΔSref, Δt2 and Δt3 the modulation of the reference signal Sref is continuously and automatically adapted to different lamps that are operated by means of the circuit arrangement. Similarly the changes in lamp properties with life time are continuously and automatically accounted for. As a result a maximal suppression of resonance is obtained for many different lamp types during their whole life time. Since the parameters determining the shape of the modulation of the reference signal Sref can be adjusted independently from each other, the shape of the modulation can be changed in many different ways resulting in practice in an even more effective suppression of the resonance than can be obtained making use of the circuit arrangement shown in Fig. 1.

Merely by way of example the functioning of the circuit arrangement shown in Fig. 2 was described for an embodiment in which the parameters ΔSref, Δt2 and Δt3 are adjusted. Of course it is possible to let the microprocessor adjust all 5 parameters or otherwise less than 3 parameters. Adjustment of more parameters will generally lead to a better suppression of the resonance.

CLAIMS:

1. Circuit arrangement for operating a high pressure discharge lamp comprising
- input terminals for connection to a supply voltage source,
- a DC-DC-converter coupled to the input terminals for generating a DC current out of a supply voltage supplied by the supply voltage source and comprising
  - a control loop for controlling the DC current at a value that is represented by a reference signal Sref,
  - a control circuit for adjusting the reference signal Sref, and
  - an output capacitor,
- a commutator for commutating the polarity of the DC current and comprising lamp connection terminals and an ignition inductor,

characterized in that the control circuit comprises means for adjusting the reference signal in dependency of the peak amplitude of an AC voltage that is present across the output capacitor and is caused by the commutation of the DC current.

2. Circuit arrangement according to claim 1, wherein the control circuit comprises circuitry for generating a signal Sring that represents the peak amplitude of the AC voltage over the output capacitor and circuitry for subtracting the signal Sring from the reference signal Sref.

3. Circuit arrangement according to claim 2, wherein the circuitry for generating the signal Sring comprises a peak detector coupled to the output capacitor.

4. Circuit arrangement according to claim 1, wherein the control circuit comprises
- a first circuit part for generating a signal Sring that represents the peak amplitude of the AC voltage over the output capacitor,
- a second circuit part for modulating the reference signal Sref at a modulation frequency that equals the frequency of the commutation of the DC current by subsequently

- decreasing the reference signal Sref by an amount ΔSref during a first time interval Δt1 that starts a second time interval Δt2 before each commutation of the DC current,
- maintaining the reference signal at the decreased value during a third time interval Δt3,
- increasing the reference signal Sref by an amount ΔSref during a fourth time interval Δt4
- a third circuit part for adjusting at least one parameter chosen from the group formed by ΔSref, Δt1, Δt2, Δt3 and Δt4 so that the amplitude of the signal Sring is minimal.

5. Circuit arrangement according to claim 4, wherein the third circuit part comprises means for increasing and decreasing the value of the parameter until the amplitude of the signal Sring is minimal.

6. Circuit arrangement according to claim 4 or 5, wherein the third circuit part comprises means for adjusting at least 2 parameters chosen from the group formed by ΔSref, Δt1, Δt2, Δt3 and Δt4 so that the amplitude of the signal Sring is minimal.

7. Circuit arrangement according to claim 6, wherein the third circuit part comprises means for adjusting the parameters ΔSref, Δt2 and Δt3 so that the amplitude of the signal Sring is minimal.

8. Circuit arrangement according to claims 4-7, wherein the third circuit part comprises a microcontroller.

ABSTRACT:

A circuit arrangement for operating a high pressure discharge lamp comprises a down converter equipped with an output capacitor and a commutator equipped with an ignition choke. The amplitude of the DC current generated by the down converter is controlled by means of a control loop. To suppress resonance of the ignition choke with the output capacitor caused by commutation of the DC current, the reference signal of the current control loop is adjusted in dependency of the amplitude of the resonance immediately before and after each commutation.

Fig. 2

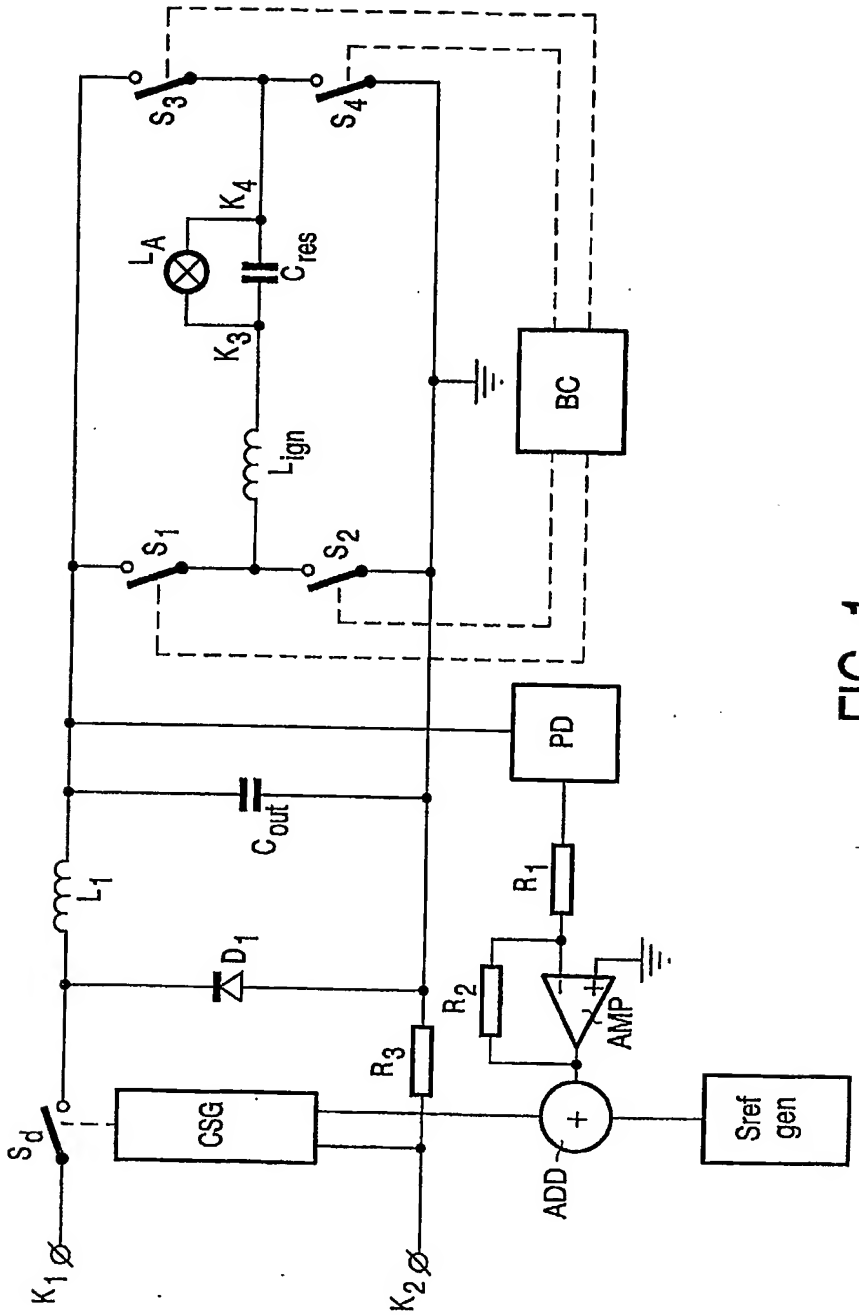

FIG. 1

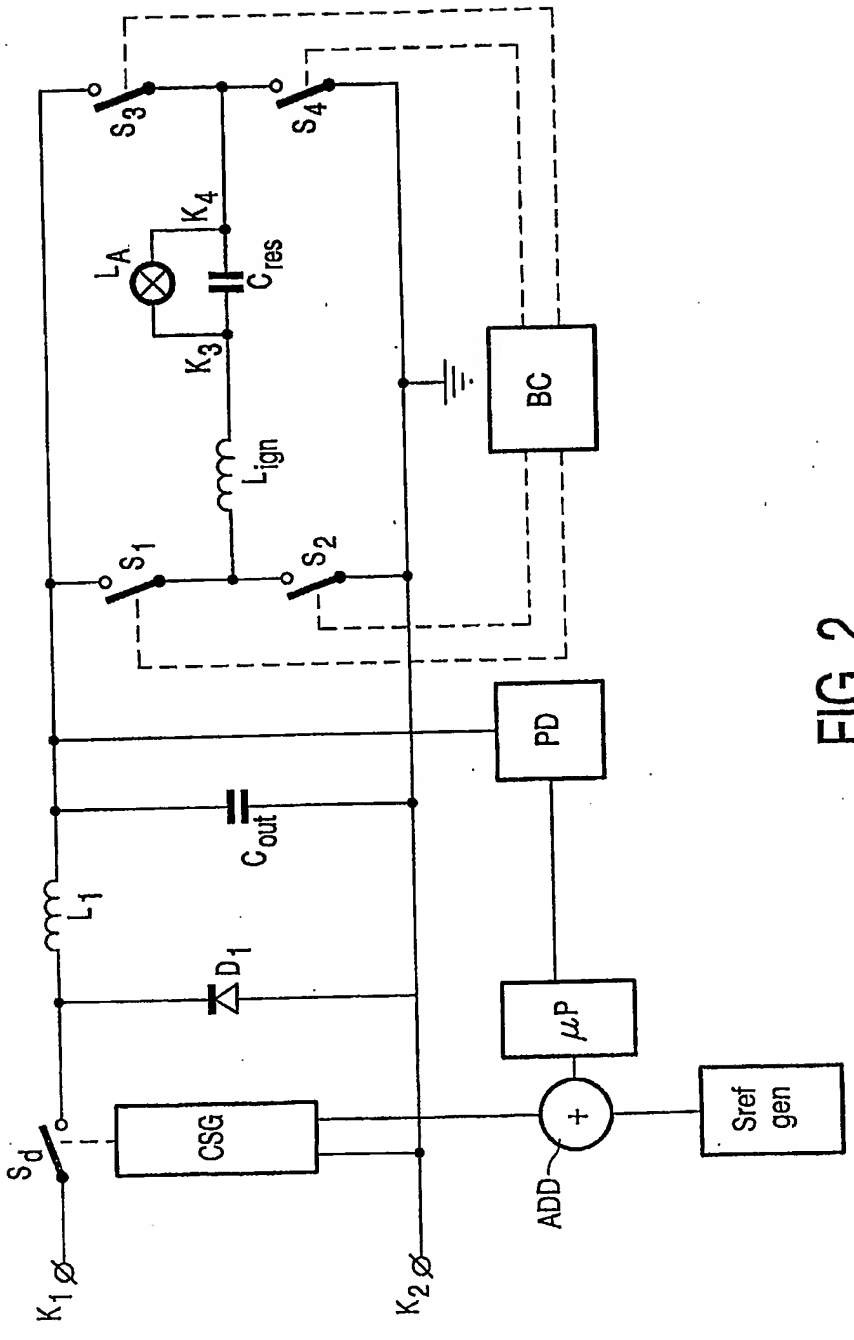
S3
S4
K4
LA
Cres
K3
Lign
BC
S1
S2
PD
Cout
L1
D1
μP
Sd
CSG
Sref gen
ADD
K1 ø
K2 ø

FIG. 2

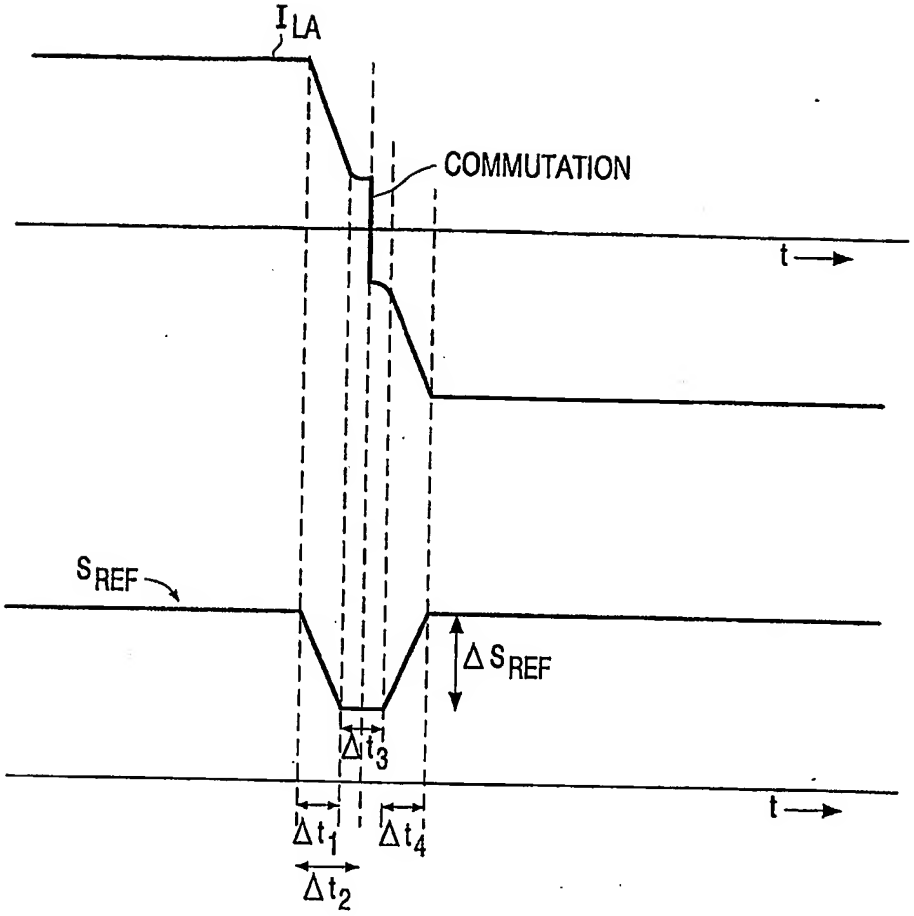

FIG. 3